

ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY
CONTROLLER COMPUTER SYSTEM

Joseph Jeddeloh

Appl. No.: Unknown

Atty Docket: MTIPAT.007C1C1

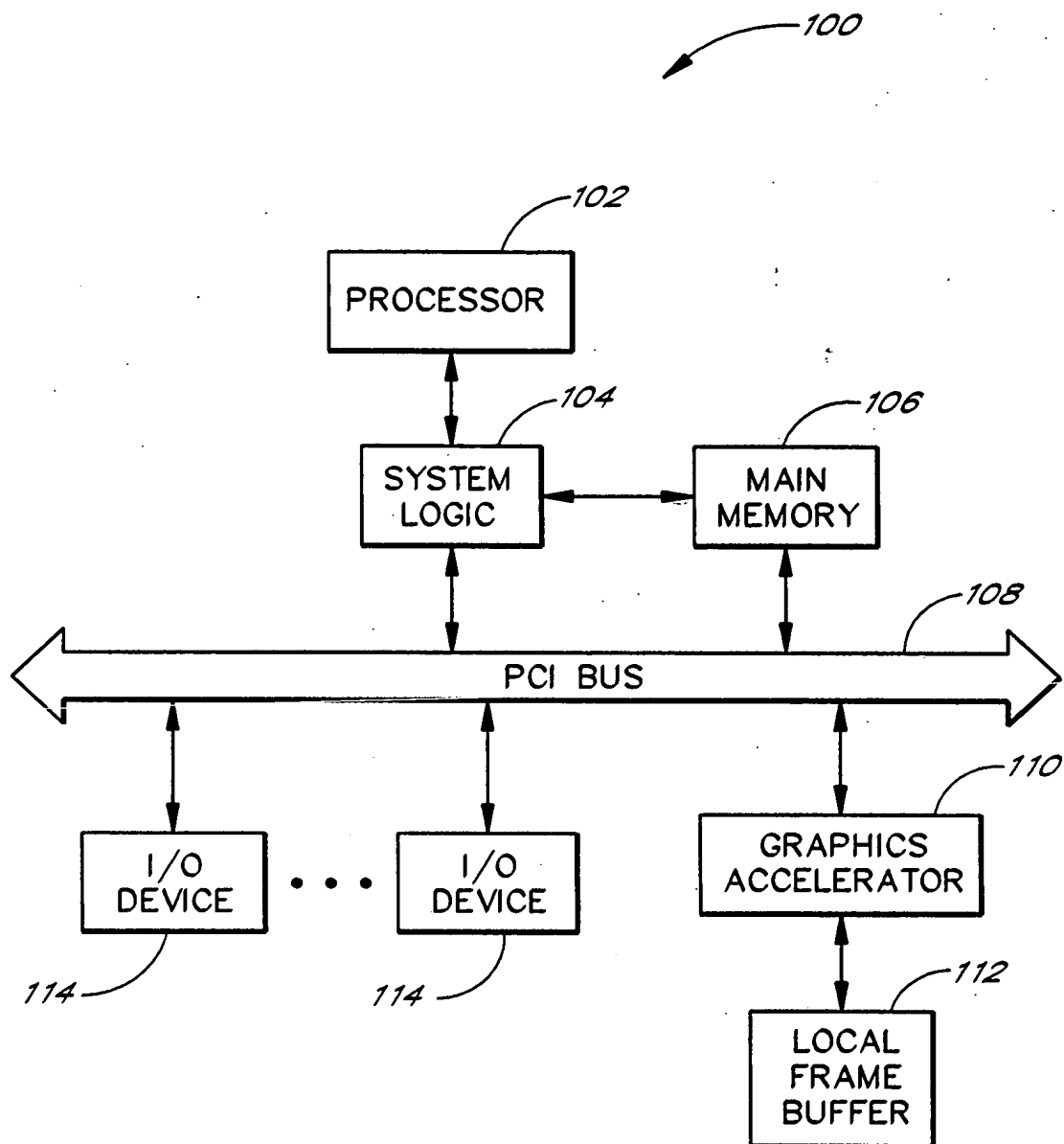


FIG. 1
(PRIOR ART)

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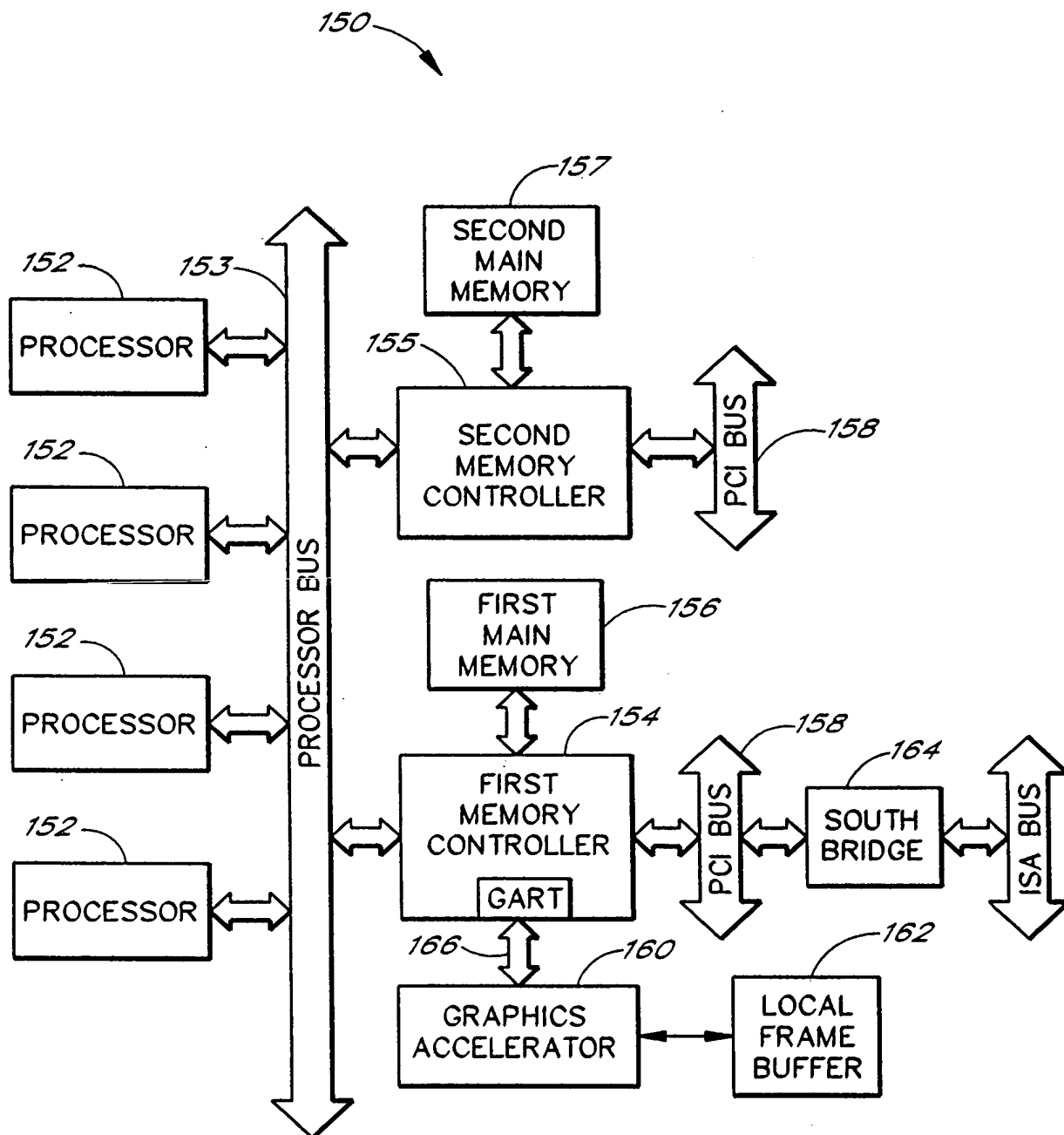


FIG. 2

ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY
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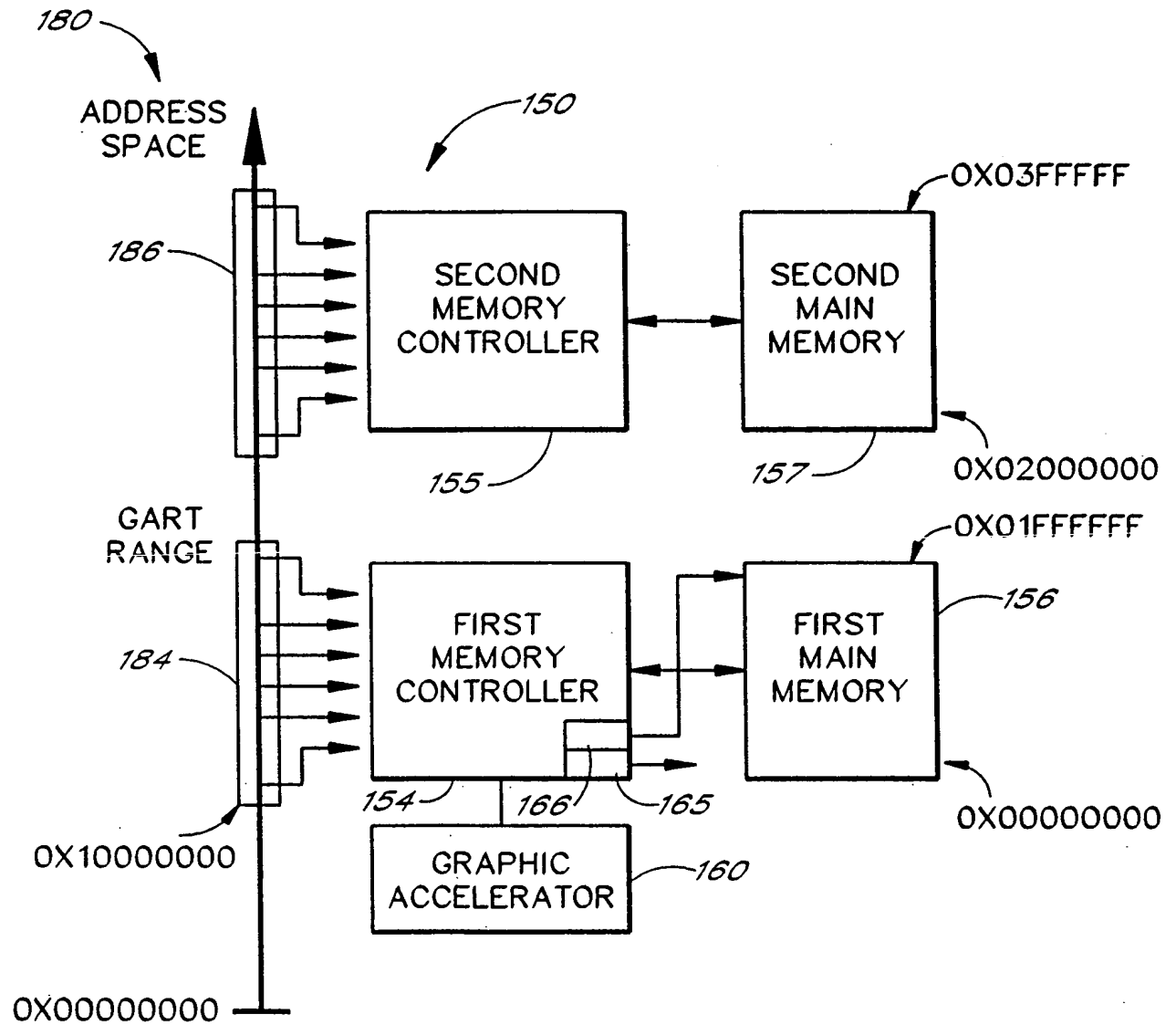


FIG. 3

ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY
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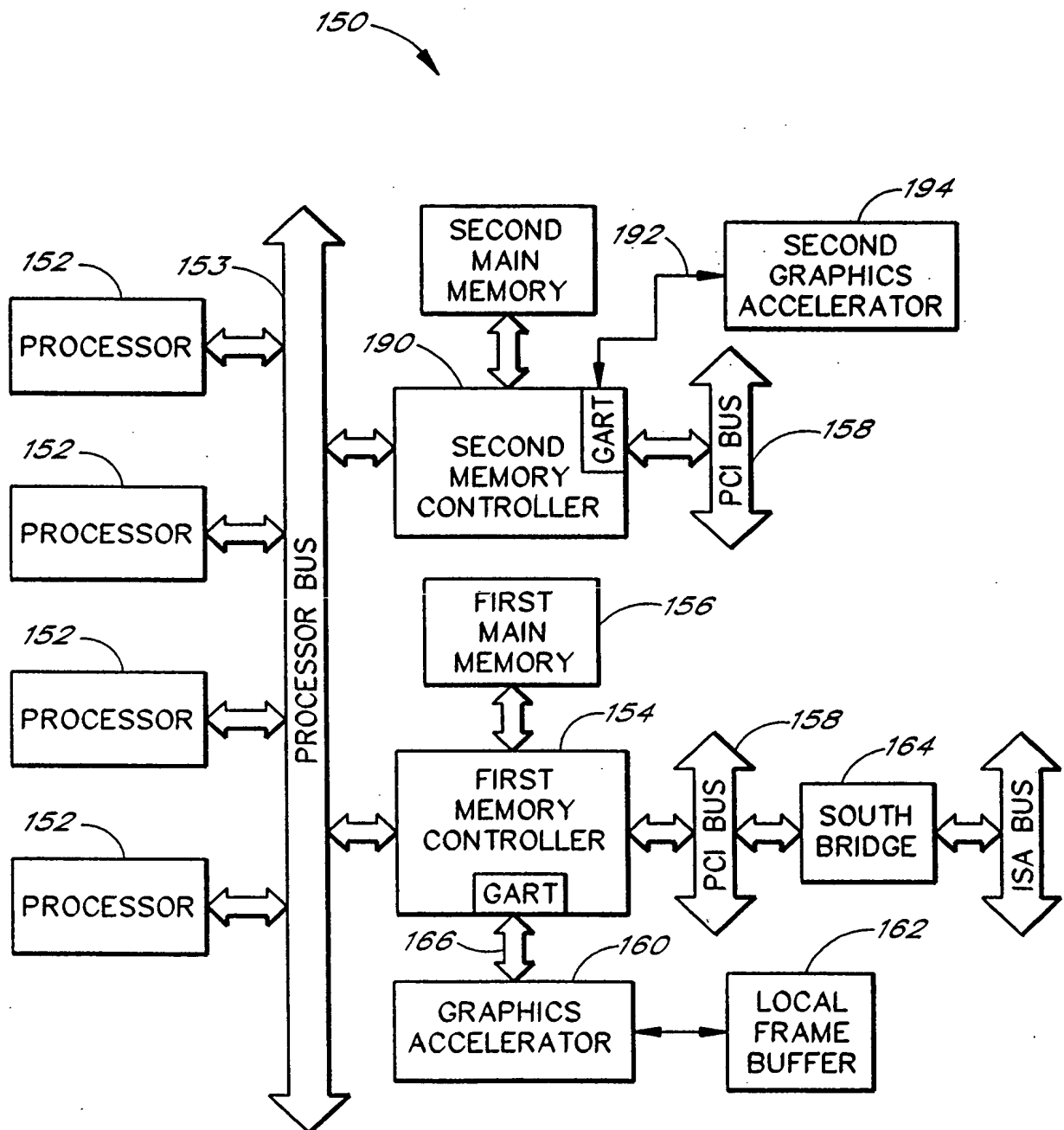


FIG. 4

ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY
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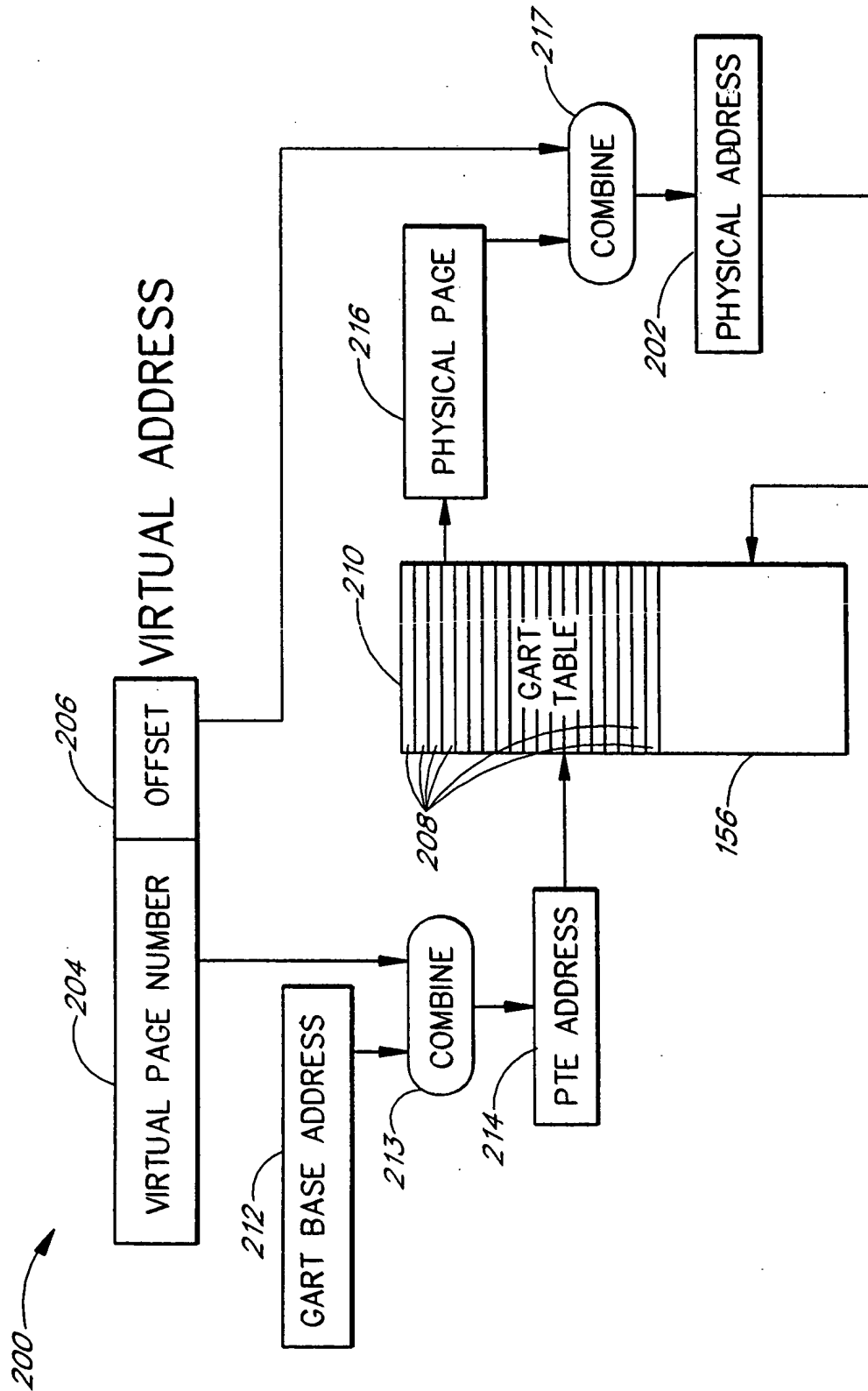


FIG. 5

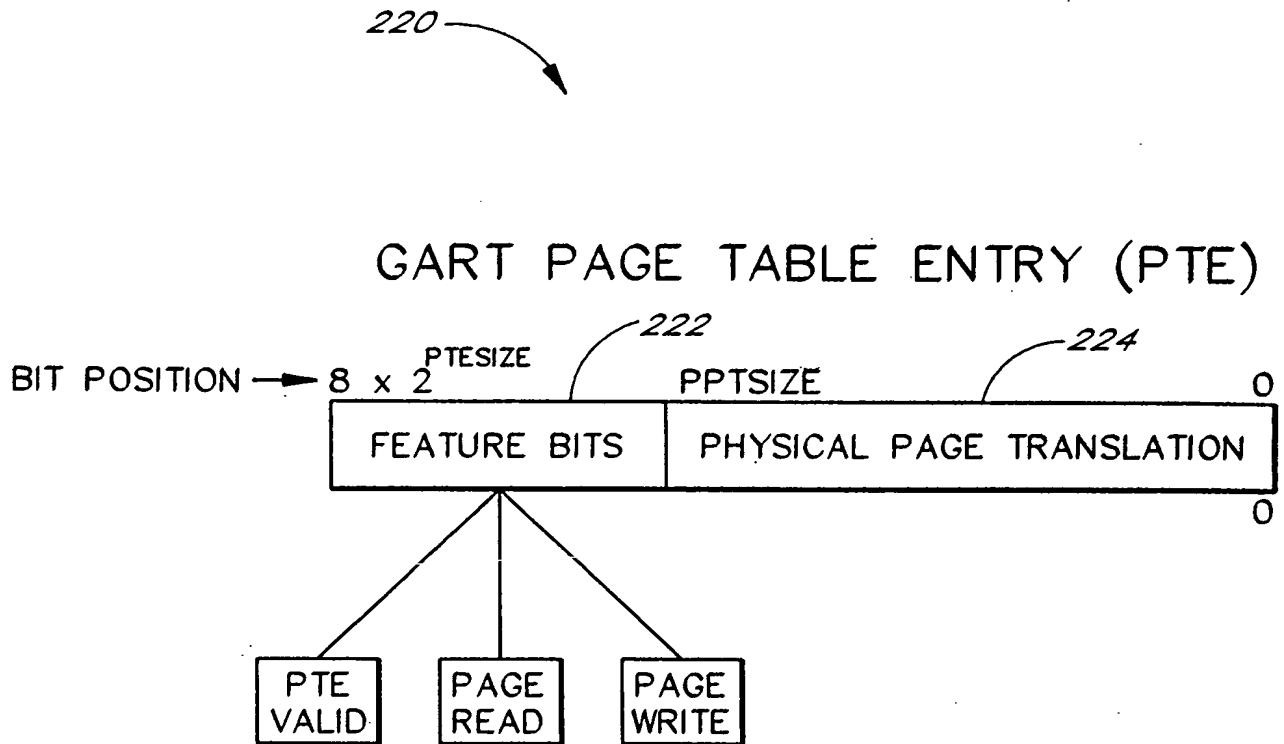


FIG. 6

